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EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,637	IMAI ET AL.	
	Examiner	Art Unit	
	Kenneth A. Parker	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-15,17-23,25-31 and 33-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-15,17-23,25-31 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/22/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

Claim 1–2, 7, 9-10, 15, 17-18, 23, 25-26, 31, 33-34, 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Shannon 5268679.

Please note that the language "over" in regards to the light shutters and sensors enables the claims to read on prior art in which all of the claimed elements are on one or two substrates and there are several substrates below (at least two), as being over then all devices are over each of substrates 1,2, and 3. The language regarding light from different sources is met if the light for those light shutters and/or sensors comes from another shutter layer, as the light through each "shutter" comes from a different source (different shutter). The use of light "source" as used in the instant specification does not appear to be used as light coming from a different emitter, but light which has come from a different place (i.e. through a different shutter). Therefore, with five stacked layers having shutters and sensors, the first shutter layer provides the claimed light sources (first, second, etc.) as the light going through the top layer of shutters. The next provides the claimed shutters which give the claimed control of the sensors, and the next gives the claimed sensors controlled by the shutters, as well as the first substrate. The next two provide the second and third substrate over which at least some of the elements are located. As Shannon has 5+ layers, it therefore meets the limitations of each independent claim. Therefore, the reference shows regarding claim

1. An electronic circuit device comprising:

a plurality of electronic circuit substrates (each 10 has wires shown) over which either of an optical shutter (each liquid crystal cell) or an optical sensor (each has a sensor) is disposed, or both of them are disposed, wherein said plurality of electronic circuit substrates comprise transparent substrates (the substrates 10 themselves), an optical signal is inputted from an external (light has to get in the device, or the shutters wouldn't do anything and the device wouldn't work, and is therefore inherent), said optical signal which has been inputted is inputted into an optical shutter or an optical sensor over a transparent substrate which is different from said transparent substrates after said optical signal has been transmitted through at least one or more of said transparent substrates, said optical shutter controls transmission and non-transmission of said optical signal (that is what the shutters do), and said optical sensor converts said optical signal into an electric signal by an electronic circuit provided over a same transparent substrate as said optical sensor (the readout matrix creates an electronic signal).

The reference shows regarding claim 2. A device according to claim 1, wherein said electronic circuit comprises a thin film transistor (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 7. A device according to claim 1, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of

transparent substrates (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 8. A device according to claim 7, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 9. An electronic circuit device comprising: a plurality of transparent substrates (each 1- has wires shown) over which either of an optical shutter (liquid crystal cell) or an optical sensor (each has a sensor) is disposed, or both of them are disposed, wherein said plurality of transparent substrates have been laminated (they are shown stacked), an optical signal is inputted from an external (it has to come from somewhere or the device wouldn't work), said optical signal which has been inputted is inputted into an optical shutter or an optical sensor over a transparent substrate which is different from said transparent substrates after said optical signal has been transmitted through at least one or more of said transparent substrates (there are many stacked), said optical shutter controls transmission and non-transmission of light (that is what shutters do), and said optical sensor converts said optical signal into an electric signal by an electronic circuit provided over a same

transparent substrate as said optical sensor (that is what sensors to, and the circuit is shown as a readout matrix).

The reference shows regarding claim 10. A device according to claim 9, wherein said electronic circuit comprises a thin film transistor (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 15. A device according to claim 9, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 16. A device according to claim 15, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 17. An electronic circuit device comprising a plurality of transparent substrates over which either of an optical shutter or an optical sensor is disposed (each 10 has wire shown and therefore has the LCD and sensor structures), or both of them are disposed, wherein an optical signal is directly inputted

into said optical shutter from an external or said optical signal is inputted into said optical shutter after said optical signal has been transmitted through said transparent substrate, in a case where said optical shutter has transmitted said optical signal, the transmitted optical signal is directly inputted into said optical sensor or inputted into said optical sensor after said optical signal has been transmitted through a transparent substrate which is different from said transparent substrates (the signals go through substrates, and strike sensors).

The reference shows regarding claim 18. A device according to claim 17, wherein said electronic circuit comprises a thin film transistor. (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 23. A device according to claim 17, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 24. A device according to claim 23, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 25. An electronic circuit device comprising: a plurality of transparent substrates over which either of an optical shutter or an optical sensor is disposed (each 10 has wire shown and therefore has the LCD and sensor structures), or both of them are disposed, wherein said optical shutter is controlled by an electronic circuit over a transparent substrate (the driving circuit is shown- see figure 1) , an optical signal inputted from an external is inputted into said optical shutter (it has to come from somewhere, so this limitation is inherent), and whether said optical signal has been transmitted or not is decided, thereby taking out an output signal of said electronic circuit (this is true by definition).

The reference shows regarding claim 26. A device according to claim 25, wherein said electronic circuit comprises a thin film transistor. (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 31. A device according to claim 25, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates. (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 32. A device according to claim 31, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is

disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 33. An electronic circuit device comprising: a plurality of transparent substrates over which either of an optical shutter or an optical sensor is disposed, or both of them are disposed (each 10 has wires for at least one of sensors and LCD shutters), wherein said transparent substrates have been laminated (they are stacked), said optical shutter is controlled by an electronic circuit provided over said transparent substrate (the driving matrix is shown), an optical signal inputted from an external is inputted into said optical shutter, and whether said optical signal has been transmitted or not is decided, thereby taking out an output signal of said electronic circuit (this is true by definition).

The reference shows regarding claim 34. A device according to claim 33, wherein said electronic circuit comprises a thin film transistor. (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 39. A device according to claim 33, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates. (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

Claim Rejections - 35 USC § 103

Claims 3-6, 11-14, 19-22, 27-30,35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shannon 5268679 in view of Yamada 5583570, Williams 5491571 Shindo et al 5738731.

Shannon shows the sensor as a photodiode (abstract), but does not indicate what level of crystallinity the circuits and photodiodes are. Note that the term "chip" is taken as met by the reference, as any circuit can be construed as chips. Yamada shows that the range of crystalline from amorphous to single crystal was applicable to photodoides "a MOSFET photocell and photodiode using a monocrystalline silicon, amorphous silicon, polycrystalline silicon or the like are known." Shindo et al shows that the higher crystallinities had higher cost and manufacturing complexity (cols 7 and 9-10). Williams shows that the higher crystalline had benefits of improved speed (column 2, lines 9-21), and therefore considering the tradeoff cost and manufacturing complexity for the higher levels of crystallinity the level of crystallinity is a result effective for the photodiode and driving circuits. It has been judicially determined that the selection of a result effective variable is at least obvious. Therefore the selection of a particular level of crystallinity, i.e. amorphous (claims 4, 12, 20, 28, 36,) polysilicon (claims 5, 13, 21, 29, 37) or single crystal silicon (claims 3, 6, 11, 14, 19, 22, 27, 30, 35, 38) would have been within the ordinary skill level, and one of ordinary skill would have found motivation, suggestion or reason to select single crystal for the best speed, amorphous

for the lowest speed but simplest manufacturing, and polycrystalline for the middle cost and speed tradeoffs for each of the photodiode and driving circuits).

Response to Arguments

Applicant's arguments filed have been fully considered but they are not persuasive. Applicant's argument is that the reference does not show the use of light from different sources. This is not persuasive, as the light at the second layer at a first shutter will come from a first source (a particular shutter above it), and light at a different shutter in the second layer will have come from a different shutter above, henceforth a different light source.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A. Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth A Parker
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Art Unit 2871